# UNCLASSIFIED

# AD 491712

# DEFENSE DOCUMENTATION CENTER

FOR

**3CIENTIFIC AND TECHNICAL INFORMATION** 

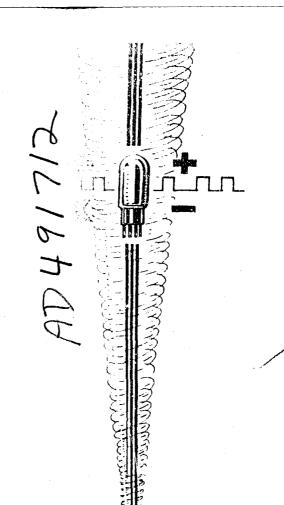
CAMERON STATION ALEXANDRIA, VIRGINIA



UNCLASSIFIED

NOTICE: When government or other drawings, specifications or other data are used for any purpose other than in connection with a definitely related government procurement operation, the U. S. Government thereby incurs no responsibility, nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use or sell any patented invention that may in any way be related thereto.

(5)



# PROJECT WHIRLWIND

Contract N50ri60 Project NR-720-003

II. TECHNICAL INFORMATION ON COMPUTER AND ASSOCIATED EQUIPMENT

c. Report R-143

SPECIFICATIONS FOR STANDARD TEST EQUIPMENT

January 18, 1949

THE SEPTION

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Сору 82



#### PROJECT WHIRLWIND

Report R-143

SPECIFICATIONS FOR STANDARD TEST EQUIPMENT

Submitted to the OFFICE OF NAVAL RESEARCH under Contract N5ori60 Project NR-720-003

Report by

Robert R. Rathbone

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts

Project 6345 January 18, 1949

#### PREFACE

During the development of the Whirlwind Computer, it became evident that the needs for testing the various component units - storage tubes, arithmetic circuits, control circuits, etc. - had a common basis in requiring certain sequences of pulses and gates. The differences in these requirements from one test setup to another were only those of frequency, amplitude, and, in a few cases, impedance level.

The Test Equipment Committee of the Project was formed to review these needs and provide a standard line of test equipment which would meet the requirements of all concerned. Such equipment would relieve the individual engineers of spending long periods of time designing their own equipment and further provide equipment flexible enough to be used as new ideas evolved in the computer program.

The equipment has been designed with maximum flexibility as its first requirement. The building-block approach enables the user to plug units together in large or small arrays as needed and to achieve a particular test setup in a few hours.

This booklet is issued as a guide to those who use the standard test equipment. It gives the performance requirements of each panel and other pertinent specification data. In addition, separate reports are being issued on each panel, giving complete circuit information, waveshapes, and typical uses.

Norman H. Taylor, Chairman Test Equipment Committee

# TABLE OF CONTENTS

	Sect
Introduction	0
Rack Power Control Panel	1
Filament Power Panel	2
Variable-Frequency Clock-Pulse Generator	3
Register Panel (A-C)	4
Gate Panel	5
<u>Coder</u>	6
Scope Synchronizer	7
Pulse Mixer	8
Pulse Standardizer	9
Delay Line Panel	
Register Panel (D-C)	
Gate and Delay	
93-Ohm Attenuator	
Cathode Follower Probe	
Video Amplifier	
Video Switch	
Holding Gun Power Supply	
Crystal Tester	
Voltage Calibrator	
Aurilianu Devices	

# SPECIFICATIONS FOR STANDARD TEST EQUIPMENT

#### INTRODUCTION

#### STANDARD TEST EQUIPMENT

#### Definition of Standard Test Equipment

Standard test equipment may be defined broadly as any non-commercial test units which have been approved by the Test Equipment Committee. At present it includes building blocks designed for specific Laboratory needs, and many auxiliary units and smaller devices used with these blocks (see list on page 2).

#### Status of Commercial Equipment

Commercial test equipment (voltmeters, tube testers, etc.) is used in quantity by the Project, but is not considered as standard. A borderline case is the Sylvania Model 5 synchroscope which has been modified to meet Laboratory specifications.

#### Standard Construction Requirements

After the need for a specific test unit has been established and the design approved by the Test Equipment Committee, a prototype is constructed. If this prototype meets operational requirements, construction of the final model is authorized. The following construction specifications must then be met:

- (1) The test unit must operate from the central laboratory power source (described on page 2).
- (2) It must fit a standard panel rack (19 inches).
- (3) Output pulses must be 0.1 microsecond at a 93-ohm impedance level.
- (4) The input and output jacks must be regulation (readily interconnectable by coaxial cable).
- (5) The appearance must be uniform, i.e., panel finish, lettering, and designation of controls, switches, jacks, etc. should be consistent with established test-equipment policy.
- (6) Each model must be numbered serially and each tube marked in order that operational data may be kept by Maintenance.

All pieces of standard test equipment (except the clocks) will eventually be provided with 3-position output switches (positive, negative, or zero output) and bus-driver crystal rectifiers in the output. This will enable the operator to mix output circuits, thus minimizing the need for pulse mixers.

#### List of Standard Units

#### Building Blocks

Variable-Frequency ClockPulse Generator
Gate and Delay
Register Panels (a-c and d-c)
Scope Synchronizer
Pulse Mixer
Coder
Gate Panel
Pulse Standardizer
Pelay Line Panel
95-Ohm Attenuator

#### Auxiliary Units and Devices

Cathode Follower Probe
Video Amplifier
Video Switch
Rack Power Control
Filament Power Panel
Holding Gun Power Supply
Crystal Tester
Voltage Calibrator
Jack Marker
Cable-Terminating Resistors
Cable-Terminating Potentiometers

#### Typical Uses of Standard Test Equipment

The equipment described in the following sections has been assembled as building blocks to perform numerous tasks. During the design of the Whirlwind computer, this method proved extremely valuable in examining the behavior of basic circuits, such as flip-flops and gate tubes, under system conditions. Even more important has been its use in testing and simulating large computer elements (storage, arithmetic registers, and arithmetic control). This application alone has saved many months in computer installation by permitting testing of one element before an associated element was completed.

The test equipment instruction booklets which are now being written present typical test setups for examining basic circuits. A separate report will be prepared describing in detail specific component tests and simulation.

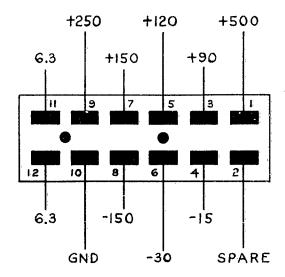
#### LABORATORY POWER SUPPLY

As one of the construction requirements for standard test equipment is to operate from the central laboratory power supplies, a description of that source is given below in order to clarify references in the specifications of each unit.

Each laboratory workbench is equipped with a power box which supplies the following voltages:

B+	Bias	Fil.
90	- 15	6.3 (a-c)
120	- 30	·
150	<b>-1</b> 50	
250		

The front panel of the box has four outlets for Jones 12-pin cable connectors, an on-off switch and red indicator light for the B+ and bias voltages, and an on-off switch and green indicator light for the 6.3 v a-c. A drawing specifying the voltages at the twelve terminals is attached to the conduit under each box, and is reproduced below.



The B+ and bias voltages (except ÷500) are fed to the power box from a central power supply source located in the basement. The +500 must be supplied by local power supply. The a-c input to the central supplies and the ±150, -15, and -30 outputs are regulated. Heinemann circuit breakers capable of switching in 1 millisecond are used in all lines and are located in remote circuit-breaker boxes. One such box can supply power to as many as six bench power boxes.

The 6.3 v a-c, supplied locally, is fed to the power box from a 20-amp transformer under the bench. Numerous 115-volt a-c outlets are provided, and an a-c circuit breaker has been installed at the main a-c entrance at each bench.

When racks of equipment are used, power is supplied through the rack power control unit described in Section 1.

#### SPECIFICATION SHEETS

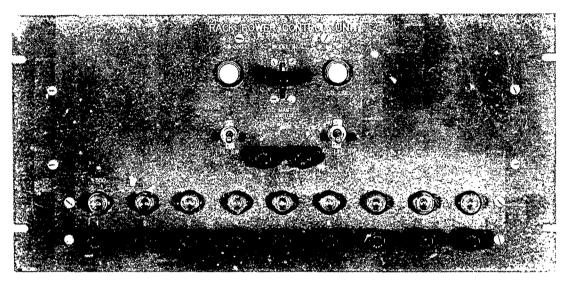
At present, this booklet does not contain specification sheets for every unit listed on page 2. Additional specification sheets are

being prepared, however, and will be distributed to all holding this report. Each sheet will have a section number in the top right-hand corner to facilitate insertion. If succeeding issues for the same equipment are necessary, the corrected sheets will bear a letter following the section number. Brief addenda or errata will be issued in memorandum form and given the same distribution.

Signed Robert R. Rathbone

Approved Jay W. Forrester

# RACK POWER CONTROL UNIT (Model 2)



#### General Description

This unit provides 6.3 v a-c and a convenient means for switching all d-c power from the central supply to equipment mounted on a standard 19-inch relay rack. When fused properly, it prevents local short circuits or overloads from tripping the main circuit breakers, thereby allowing other racks to continue drawing power. In addition, the equipment has a time-delay relay which acts as a current-surge suppressor by shorting out series resistors in the +250 and +150 lines.

#### Specifications

Dimensions:  $8 \frac{3}{4} \times 10 \times 19$  inches.

Input (rear chassis): D-C input from bench power box through a 12-pin male Jones plug.

115-v, 60-cycle input through a flush motor plug.

Output (rear chassis): Standard d-c voltages (central power supply) to 4 female 12-pin Jones plugs.

6.3 v a-c (40 amp) from 2 filament transformers (primaries tapped). Output from one through the 4 Jones plugs; output from the second (with center taps) brought out to 2 terminal strips.

4 115-v a-c outlets on top rear of chassis.

Auxiliary Power: Filament Power Panel (Sect. 2) may be plugged into the 115-v a-c outlet marked "AUX. FIL" if additional filament power is needed.
+500 v may be fed into the unit through the Jones-plug input or a uhf coaxial jack (J2).

Maximum Loads: 2 amp for d-c voltages
15 amp for 115 v a-c
80 amp for 6.3 v a-c
(80 amp additional with Fil. Power Panel)

# Fusing (front panel):

(1) D-C voltages - 3AG fuses up to 2 amp.
(2) 115 v a-c - 4AG fuses, 15 amp, on both sides of line.

## Controls (front panel):

(1) Multi-contact D-C MASTER SWITCH.

(2) Toggle Switch for a-c input, A-C LINE.

- (3) FIL. SWITCH, toggle switch controlling primary power to both fil. transformers and to 115-v a-c outlet, AUX. FIL.
- (4) Current-surge suppressor. Time-delay relay, energized by d-c master switch, cuts out series resistors in +250 and +150 lines. Optimum delay 8 seconds.

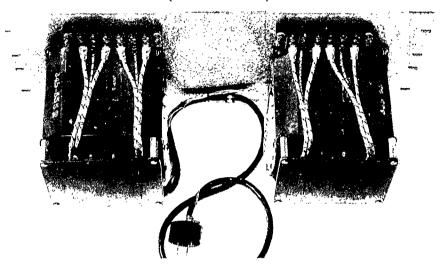
# Indicators (front panel):

A-C line - Drake 60N Red Jewel
Fil. - Drake 60N Green Jewel
D-C (all) - NE51 neon lamps except -15 v, -30 v which use incandescent lamps.

#### References

Engineering Note E-118 Circuit Schematio D-39467-1

# FILAMENT POWER PANEL (Models 1 & 2)



#### General Description

This unit is used to supply auxiliary filament power when the amount from the rack power control unit is inadequate for test setups. It consists of two 40-amp filament transformers mounted on the rear of a panel. Model 1 is the same as Model 2 except that the transformers of the latter each have two center-tapped secondaries instead of four.

#### Specifications

Construction: Panel for rack mounting.

Dimensions:  $8 \frac{3}{4} \times 19$  inches.

Transformers: Two 40-amp, 6.3-v a-c filament transformers.

Each transformer has two center-tapped 20-amp secondaries (Mod. 2), four center-tapped 10-

amp secondaries (Mod. 1).

Input: 115-v a-c primary power from AUX. FIL. outlet

on rack power control unit, controlled by

fil. switch.

Output: Secondaries with center taps brought to Jones terminal strips on rear of panel. May be used

in parallel to obtain more than 20 amp on one

line.

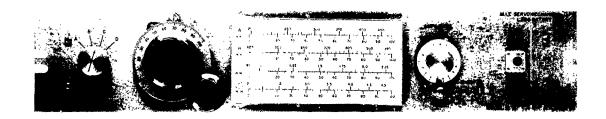
### References

43

Circuit Schematic B-39759 (Model 1) B-40127 (Model 2)

Engineering Notes E-117 (Model 1)

# VARIABLE-FREQUENCY CLOCK-PULSE GENEFATOR (Model 2)



#### General Description

This unit is a primary pulse source for test setups of gate tubes, flip-flops, matrices, bus drivers, control-line drivers, and other components. It is also a basic building block for complete systems and special tests, providing standard output pulses 0.1 microsecond long at a 93-ohm impedance level with frequencies variable from 0.2 to 4.9 megacycles.

#### Specifications

Construction: Panel and chassis for standard rack mounting.

Dimensions:  $3\frac{1}{2} \times 5\frac{1}{2} \times 19$  inches.

Circuits: 6SN7 cathode-coupled oscillator.

6AG7 inverter. 6L6 R-L-C peaker. 6L6 buffer amplifier.

Output: 0.1-usec half-sine-wave positive pulses at

93-ohm impedance level.

Amplitude Control: 0 to 40 volts, control linear but not

calibrated.

Frequency Range: 0.2 to 4.9 megacycles in 4 bands. Calibra-

tion chart on front panel.

Frequency Stability: 20 parts in 1,000,000.

Power Requirements: (standard laboratory power supply)

+250 v, 130 ma (maximum) -150 v, 1.3 ma 6,3 v a-c, 3.05 amp

#### References

Circuit Schematic: B-39735-1 Instruction Booklet: Report R-144 Specification of Components: PL 39735 REGISTER PANEL
(a-c coupled)



#### General Description

The register panel contains a d-c flip-flop, a gate tube a-c coupled through a cathode follower to one of the FF plates, two indicator circuits, a complementing input, and set and clear inputs (one input and zero input respectively). It provides two gate outputs from the flip-flop in addition to a gated-pulse output. The register panel is used for system mock-up, counting, synchronizing, and pulse distribution.

#### Specifications

Construction: Panel and chassis (5 x  $5\frac{1}{2}$  x 19 inches).

Circuits: Trigger tube (7AD7) to pulse FF common cathode

connection.

Trigger-tube-input mixer (2 channels).

0-input inverter ( $\frac{1}{2}$  6J6) to pulse FF grid.

1-input inverter ( $\frac{1}{2}$  6J6) to pulse FF grid.

2 inverter-input mixers (3 channels each).

2 cathode followers from FF plates (each \( \frac{1}{2} \) 5687). Gate tube (7AK7) a-c coupled to the 1 side of FF.

Buffer emplifier (7AD7) for gated pulse.

Indicator tube (6J6).

2 R-C integrating circuits to indicator tube.

Input:

Standard 0.1-usec half-sine-wave positive pulses -

- (a) To TT input.
- (b) To No. 1 grid of gate tube.

- (c) To the O inverter.
- (d) To the 1 inverter.

#### Input Amplitudes:

- (a) To trigger tube and FF -10 v min. (to obtain specified output amplitude range), 20 v max.
- (b) To gate tube 14 v min. (to obtain specified output amplitude range), 35 v max.

#### Resolution Time:

0.25 µsec min. for trigger tube, and flip-flop. 0.33 µsec min. for gate tube.

#### Output:

Gated pulse

Half-sine-wave pulse, approx. 0.1 µsec. Amplitude adjustable from 6 to 23 v. Polarity reversible. Minimum delay through gate circuit 0.06 µsec.

#### Gates

O gate and 1 gate. Amplitude 22 v from cathode follower. Coupling to external gate tubes by coaxial cable. Rise and fall times 0.2 usec.

#### Visual Output

O and 1 neon indicator, lamps (1/25 watt) to show content of FF.

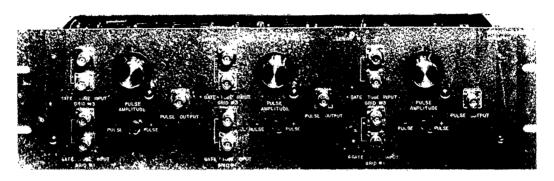
### Power Requirements: (standard laboratory power supply)

+250 v, 4 ma + 90 v, 2.5 ma +150 v, 120 ma 6.3 v a-c, 5 amp +120 v, 7 ma - 15 v, 36 ma

#### References

Block Schematic: A-39903-1 Circuit Schematic: B-39754-1 Instruction Booklet: Report R-145 Specification of Components: PL 39754

#### GATE PANEL



#### General Description

The gate panel consists of three independent gate tubes and associated buffer amplifiers. The No. 3 grid of each gate tube is connected to paired jacks on the front panel so that externally generated gates can be utilized. The No. 1 grids also have paired input jacks for pulses to be gated. The polarity and amplitude of the output pulse can be selected by panel controls.

The gate panel was designed to provide auxiliary gate-tube circuits for the register panel (a-c or d-c). In applications where steady-state gate pulses are used, the gates can be obtained from the gate and delay unit.

#### Specifications

Construction: Panel and chassis for standard rack mounting.

Dimensions:  $5 \times 5\frac{1}{2} \times 19$  inches.

Circuits: 3 7AK7 gate tubes.

3 7AD7 buffer amplifiers.

Input: External gates

Paired input jacks to the No. 3 grid of each 7AK7.
O.l-microfarad coupling condenser extends lower

repetition frequency range of gate.

Switch for selecting input from a-c or d-c register

panel.

Pulses to be gated Paired input jacks to No. 1 grid of gate tube.

Input pulse must be positive.

Input Amplitudes:

Min. 14 v, (to obtain specified output amplitude

range) max. 35 v.

Output:

Gated pulses

Each gate tube has a single output jack.

Polarity reversible.

Amplitude control in cathode of 7AD7, 6 to 23 volts.

Minimum Deray: (all sections) 0.06 µsec.

Resolution Time: (all sections) 0.33 µsec.

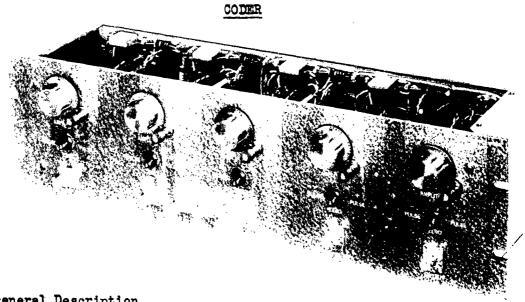
Power Requirements (all sections):

Voltages	Current with no signal	Current with 1-mc clock pulses
+250 <b>v</b>	1.2 ma	17.0 ma
+150 <b>v</b>	1.5 ma	6.1 ma
+ 90 <b>v</b>	0.5 ma	8.3 ma
- 15 v	Ö	2.2 ma
6.3 v a-c	4.2 amp	4.2 amp

#### References

Circuit Schematic: C-32496

Instruction Booklet: Report R-151



#### General Description

The coder is principally used for system testing and mock-up. Two of its functions have been to store binary numbers and to simulate the pulse-distribution element of control, i.e., reading numbers into arithmetic registers and presetting a step counter. It is also useful for feeding several units which may require different input amplitudes.

The coder will deliver up to five O.1-microsecond half-sinewave output pulses for a single input pulse. A three-position toggle switch at each output provides a positive pulse (position 1), zero output (position 2), and a negative pulse (position 3). The operator may then set up whatever five-digit binary code may be required for a specific operation.

#### Specifications

Dimensions:  $4-1/2 \times 5 \times 19$  inches.

Circuits: 6AG7 inverter.

Two 6AC7's in parallel as an RLC peaker.

Five 6AG7 buffer amplifiers.

The inverter-peaker circuit is used as a pulse standardizing circuit with a resolving time of 0.5 microsecond for 0.1-microsecond pulses.

Imput: Single input, paired jacks. Input pulse must be

positive and have at least a 12-volt amplitude to obtain full range of output. Max. input 50 v. Resolution Time: 0.5 µsec (all sections).

Minimum Delay: 0.05 µsec (through all sections).

Output: Five single output jacks. Each output

has a 3-position toggle switch for positive and negative pulses, or zero output. Amplitude of each output

variable from 4 to 19 volts.

Power Required: (1-mc pulses, steady state):

<b>Voltages</b>	Currents		
	No Sig.	Signal	
+250 v d.c.	4.7 ma	57 ma	
+150 v d.c.	83 ma	70 ma	
+120 v d.c.	20 ma.	17 ma	
- 15 v d.c.	O me.	0.2 ma	
6.3 v a.c.	5.2 amp	5.2 amp	

#### References

Memorandum: M-440

Circuit Schematic: D-32590

#### SCOPE SYNCHRONIZER



#### General Description

The scope synchronizer is used in conjunction with a synchroscope to view high-frequency pulse sequences. By dividing the high frequencies to some value between 0.5 and 30 kc, it produces positive pulses suitable for triggering the synchroscope. The unit provides two methods for adjusting the delay of its output pulses, and has a control for output amplitude.

#### Specifications

Construction: Panel and chassis

Dimensions:  $3\frac{1}{2} \times 5\frac{1}{2} \times 19$  inches.

Circuits: (all tubes type 5687).

2 synchronized multivibrators.

Delay multivibrator.

R-L-C Peaker (output circuit).

Input: Input pulse must be positive, prf between 500

cycles an 6 megacycles. No. 1 input jack for

frequencies above 500 kg. No. 2 jack for

frequencies below 500 kc.

Output: Positive half-sine-wave pulse, 0.5 µsec long.

Amplitude variable from 0 to 175 volts. Output should be coupled with unterminated

cables.

Pulse may be delayed from 5-15 µsec by either smooth delay control or sync delay (trailing edge of gate synchronous with an input pulse, delay in steps equal to time between pulses).

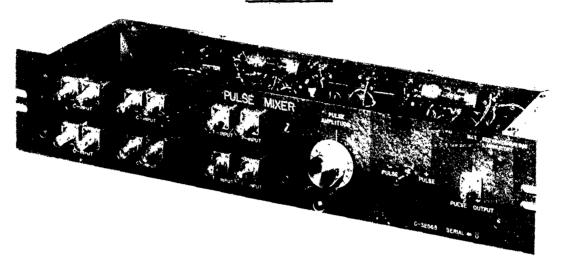
# Power Requirements: (standard laboratory power supply)

+150 v 96 ma -150 v 1.3 ma 6.3 v a-c 3.6 amp

### References

Circuit Schematic: B-39822 Engineering Notes: E-126

#### PULSE MIXER



#### General Description

The pulse mixer can take pulses from as many as 8 external lines, mix them into a pulse standardizing circuit, and produce a single chain of standard pulses. A major use of the equipment is to mix numerous external pulses intended to trigger the same flip-flop.

#### Specifications

Construction: Panel and chassis.

Dimensions:  $3\frac{1}{2} \times 4\frac{1}{2} \times 19$  inches.

Circuits: 7AD7 inverter 6AG7 RLC peaker

6AG7 buffer amplifier

The inverter-RLC peaker circuit is employed as

a pulse standardizing circuit.

Input: 3 input channels mixed into 7AD7 inverter. 4 channels present high impedance and are provided

with paired jacks to enable termination or continuance of incoming line. Remaining 4 channels utilize 3:1 step-up transformers so that the unit may be driven directly from gate tubes. Input pulses must be positive. Min. amplitude 12 volts to obtain full output range;

max. amplitude 50 volts.

Resolution Time: 0.5 µsec.

Output: Standard 0.1-usec output pulses. Pulse

polarity reversible. Output amplitude

variable from 12 to 35 volts.

Minimum Delay: (through unit) 0.08 µsec.

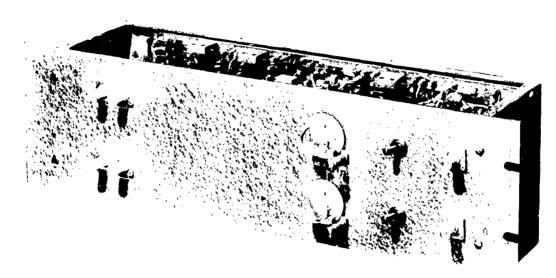
Power Requirments (1-mc pulses, steady state):

	No Sig.	Signal
+250	0.4 ma	16 ma
+150	47 ma	44 ma
+120	13 ma	12 ma
- 15	16 ma	16 ma
6.3 v a-c	1.9 amp	

#### References

Circuit Schematic: C-32565-2 Memorandum: M-458

#### PULSE STANDARDIZER



#### General Description

The pulse standardizer is used to convert positive pulses of different amplitudes and shapes to standard 0.1-usec half-sine-wave pulses whose amplitude and shape are independent of the imput amplitude and shape. It is used to provide standard pulses for test equipment, computer components, and for making measurements on basic circuits. The unit is constructed in duplicate on a single panel and chassis.

#### Specifications

Dimensions:  $4-1/2 \times 5-1/2 \times 19$  inches.

Circuits: 5687/2 buffer amplifier

5687/2 inverter 6AG7 RLC peaker

6AG7 buffer amplifier

Imput (each unit): 2 parallel jacks.

Input pulse must be positive, but amplitude may vary from 12 v min. to 50 v max. Resolution time: 0.45 µsec.

Output (each unit): Standard O.1-µsec pulse. Polarity

reversible. Amplitude range 12 to 35 volts, controlled by potentiometer in final buffer. Bus-driver crystal

rectifier in output.

# Minimum Delay (through each unit): 0.1 µsec

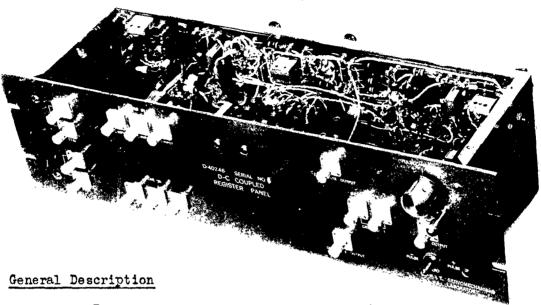
# Power Requirements (both units):

Voltages	Currents	
	No Sig.	1-mc pulse
+250 v d.c.	1.75 ma	25 ma
+150 v d.c.	105.0 ma	175 ma
- 15 v d.c.	30 ma	30 ma
6.3 v a.c.	4.4 amp	4.4 amp

# References

Circuit Schematic: C-33001

# REGISTER PANEL (D-C Coupled)



The d-c coupled register panel contains a flip-flop, a gate tube d-c coupled to the flip-flop through a buffer amplifier, and associated circuits. In appearance, it closely resembles the a-c coupled register panel described in Section 4. Functionally, it can be put to more general use, differing from the a-c model in that its flip-flop can remain in either the 0 or 1 position for any length of time. This important characteristic, made possible by the d-c coupling between flip-flop and gate tube, eliminates the need for complementing the flip-flop periodically with pairs of restorer pulses, as is required when the a-c model is used at low frequencies.

#### Specifications

Construction: Panel and chassis.

Dimensions:  $5 \times 5 \frac{1}{2} \times 19$  inches.

Circuits: Trigger tube 656 (both halves in cascade

as an inverter-limiter).

Trigger-input mixer (2 channels).

0-input inverter (1/2 6J6). 1-input inverter (1/2 6J6).

Two inverter-input mixers (3 channels each). Flip-flop (2 6AN5's). Two 6AN5 buffer amplifiers for flip-flop. Gate tube (7AK7). Buffer amplifier (7AD7). Indicator tube (6J6).

#### Input: 0.1-usec half-sine-wave positive pulses:

- (a) To TT input (2 mixer channels).
- (b) To No. 1 grid of gate tube.
  (c) To the 0 input) 3 mixer channels each.
  (d) To the 1 input)

# FF Resolution Time: 0.33 microsecond (minimum).

#### Output: Output pulse from gate tube:

Half-sine-wave, approx. O.1 microsecond. Amplitude adjustable from 8 to 30 volts. Polarity reversible.

#### Gate from Flip-Flop:

O-gate and 1-gate outputs. Amplitude 20 volts. Will feed 93-ohm unterminated line.

#### Visual Output:

O and I neon indicator lamps to show state of flip-flop. External terminals provided for remote indicator lights.

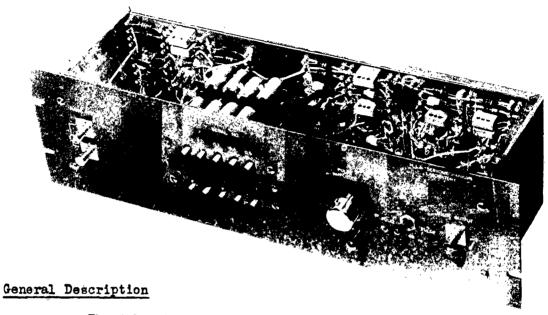
#### Power Requirements:

Voltages	Qurre	nts
	No Sig.	1-mc input to TT
+250 v d.c.	2 ma.	2 ma.
+150 v d.c.	14 ma	20 ma
+ 90 v d.c.	0 ma	O ma.
-150 v d.c.	125 ma	112 ma
- 15 v d.c.	56 ma	55 ma
6.3 v a.c.	4.75 amp	4.75 amp

#### References

Instruction Booklet: Report R-171 Circuit Schematic: D-40246

#### DELAY LINE PANEL



The delay line panel is used to delay 0.1-microsecond pulses, in steps of 0.1 microsecond, up to a maximum of 1 microsecond. External terminals are provided for adding extra delay lines.

### Specifications

Dimensions:  $41/2 \times 51/2 \times 19$  inches.

Delay: 9 delay lines, each 0.1 µsec.

Inherent delay of unit 0.1 µsec.

Terminals on rear of chassis for additional delay

lines.

Circuits: 6AG7 input buffer amplifier.

9 delay lines, each 0.1 µsec 1100 ohms, can

be switched in series. 1/2 5687 buffer amplifier.

1/2 5687 inverter. 6AG7 R-L-C peaker.

6AG7 output buffer amplifier.

Input: Positive 0.1-\musec half-sine-wave pulse.
Minimum pulse amplitude 8 volts.
Resolution time of equipment 0.45 \musec.

Output: 0.1-usec pulses, polarity reversible, amplitude variable up to 36 volts with a 15-volt input pulse. Output circuit is transformer coupled to match 93 ohms.

### Power Requirements:

<b>Voltages</b>	Currents	
	No Sig.	I-me input
- 15 v d.c.	28 ma	25 ma
+120 v d.c.	ll ma	11 ma
+150 v d.c.	46 ma.	62 ma
+250 v d.c.	9 ma	29 ma
6.3 v a.c.	2.85 amp	2.85 amp

### References

Photograph: F-689 Circuit Schematic: D-40307



### General Description

The purpose of the gate and delay unit is to provide a test equipment building block which can supply a gate pulse, a delayed pulse, or both, to external test blocks or complete systems.

#### Specifications

Dimensions: length - 19 inches width - 5 1/2 inches depth - 6 1/4 inches

Circuits (duplicate sections): 6AK5 trigger tube.

1/2 5687 delay multivibrator. 616 cathode follower.

6L6 R-L-C peaker. Lb buffer amplifier

Imput (each section): 0.1-usec half-sine-wave positive

pulses of at least 20 volts amplitude.

Output (each section): Unclipped gate:

Amplitude +40 volts. Rise time 0.2 µsec. Fall time 0.1 µsec.

Clipped gate -

Rise time 0.3 µsec.

Fall time 0.1 µsec.

Gate length continuously variable from 0.5 µsec to 2500 µsec in four overlapping ranges.

Delayed (output) pulse:

0.1-µsec half-sine-wave pulse across a 93-ohm

Pulse amplitude is continuously variable from O to approximately 40 volts.

Polarity reversible.

Delay time equal to gate length.

Resolution Time: For coarse delay setting of 10 µsec: 1 µsec.

50 μsec: 2 μsec. 450 μsec: 10 μsec.

2500 µsec: 70 µsec.

Power Requirements: (both sections)

Voltages	iges Çurr	
<del></del>	No Sig.	4-kc Signal
+250 v d.c.	115 ma	110 ma
+150 v d.c.	220 ma	195 ma
-150 v d.c.	8.5 ma	8.5 ma
6.3 v a.c.	7.55 amp	7.55 amp

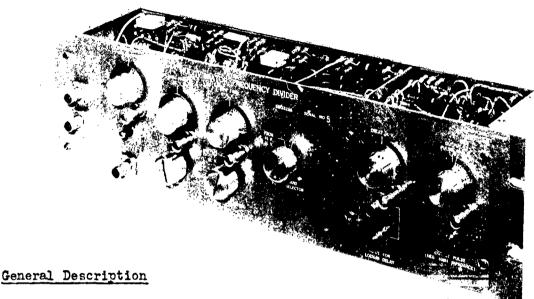
Voltage Regulation:

The voltages of the multivibrator are filtered sufficiently to allow operation with an unregulated power supply which is reasonably stable. Any low-frequency variations, of the order of 5 cps, in the power supply will change the delay time of the unit.

#### References

E-121 Engineering Note: Circuit Schematic: D-37148 Photograph:

#### MULTIVIBRATOR FREQUENCY DIVIDER



The unit is a pulse generator covering a range from 200 kc to 60 cps and which may be synchronized with any frequency equal to or greater than the output frequency. Two output pulses are provided; one a standard 0.1-usec pulse, the other a high-impedance negative pulse used to trigger a synchroscope.

#### Specifications

Dimensions:  $51/4 \times 6 \times 19$  inches, for rack mounting.

Circuits: 2 input pulse amplifiers (each 1/2 5687).

High-freq. multivibrator (5687). Low-freq. multivibrator (2051).

Pulse generator for 0.1-usec pulses (1/2 5687).

Delay multivibrator (5687).

Output amplifier for 0.1-usec pulses (6AG7). Output amplifier for high-impedance pulses

(1/25687).

Input to Dividers: Input pulses - positive, 0.1 µsec or longer.

Pulse amplitude - 15 v min. PRF - 60 cps to approx. 5 mc.

Multivibrator ranges overlap between 2.5-3 kc.

Input to Lock-in Delay: For synchronized delay, pos-

itive pulses may be fed to this input. These are amplified and fed to the delay multivibrator.

Standard Pulse Output:

0.1-usec half-sine-wave pulses, polarity reversible; amplitude adjustable up to 25 v when output feeds a 93-ohm terminated line.

Output Pulse (Neg. High Impedance): 0.2-µsec leading

edge, amplitude adjustable up to 100 volts. Will drive an unterminated 93-ohm line of reasonable length. Occurs at the end of a delay interval variable from 5 to 100 µsec.

Power Requirements:

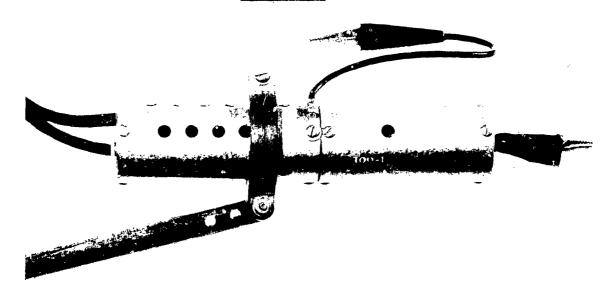
+250 v d.c. at 115 ma +150 v d.c. at 6.4 ma -150 v d.c. at 8.4 ma 6.3 v a.c. at 4.5 amp

#### References

Engineering Note: E-281 Circuit Schematic: D-33285 Photograph: F-1301 Report R-143

Sect. 14

#### VIDEO PROBE



#### General Description

The video probe is used in conjunction with a video amplifier and synchroscope to permit pulse measurement and observation. It is designed to feed a terminated cable having a characteristic impedance of 93 ohms. The cable may be up to 100 feet in length without introducing reflections.

#### Specifications

Construction: The probe is 7 inches long and 1 1/2

inches in diameter, and has two sections: the attenuator and cathode follower.

Each section is encased in brass tubing to provide shielding against hand capacitance and pickup of stray voltages. A "unipod" overcomes the difficulty of using the probe

to test a vertical panel.

Input: Signal amplitude + 1.8 volts max., + 0.15

volt min. (both determined by video

amplifier).

Gain: Approximately 1/3.

Sect. 14 Page 2

#### Circuits:

The cathode-follower circuit has a highfrequency response usable to 50 megacycles, an input impedance level of 10 megohms within the usable range, and an output impedance of 93 ohms. A type CS-968 subminiature triode was selected because of the tube's small size, high mutual conductance, and high dissipation ratings. Since the tube overloads at voltages greater than 1 or 2 volts at the input, plug-in attenuators are provided so that a wide range of input voltages can be accommodated. These attenuators include 10:1, 30:1, and 100:1 types; all have input impedance representable by a resistance of 10 megohms shunted by a capacitance of 2 to 8 micromicrofarads.

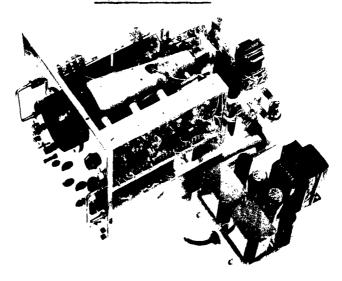
#### Power Supply:

If the probe is used near its video amplifier and synchroscope, power is obtained from a supply mounted on the synchroscope chassis; if it is used at a remote distance from the synchroscope and amplifier, a portable power supply is available. Voltages used are +75 v d.c. and 6.3 v a.c.

#### References

Instruction Manual: R-104
Circuit Schematic: B-33328
Power Supply Schematic: B-33410
Attenuator Schematic: B-33401

#### VIDEO AMPLIFIER



### General Description

The video amplifier is a wide-band amplifier constructed to fit inside the cabinet of a commercial synchroscope. It is used with a video probe and synchroscope to permit pulse measurement and observation.

#### Specifications

Circuits: First stage - input amplifier (6AH6).

Second stage - push-pull phase inverter (2-6AH6's).

Third stage - push-pull amplifier (2-6AH6's).

Fourth stage - push-pull driver amplifier (2-6AH6's).

Fifth stage - push-pull final amplifier (829-B).

#### Design Characteristics:

Frequency response:  $\pm 1$  db: 25 cps to 20 mc. -3 db points: 17 cps and 28 mc.

Transient and test response:

Amplifier rise time (from 10 to 90%) 0.013 μsec. Maximum square-wave droop: 5% in 600 μsec. Half-sine-wave pulse 0.07 μsec long decreased in amplitude 5%.

#### Input:

Input-signal amplitude approximately 0.05 peak-to-peak volt minimum (depending on vertical sensitivity of scope tube); approximately 0.6 peak-to-peak volt maximum (depending on linearity requirements).

#### Input circuit:

33,000 ohms shunted by 17-µµf stray capacitance. Grid coupled to 1-µf 200-volt condenser. Probe cable is terminated by a 25-ohm gain-control potentiometer in series with a 68-ohm resistor.

#### Output:

Output voltage 120 to 150 peak-to-peak volts. Over-all gain 45 db.

Power Suppl	ly: Voltages	Currents
	-225 v d.c.	230 ma
	+180 v d.c.	200 ma.
	6.3 v a.c.	6 ஹாற
	6.3 v d.c.	450 ma

#### Construction:

#### Mounting:

Chassis,  $5 \times 6 \times 14$  inches, mounted vertically, one end flush to synchroscope panel. Wiring is accessible for testing.

#### Power supply:

Constructed on separate chassis, not mounted inside synchroscope cabinet. Connected to amplifier by power cable; unregulated.

#### Controls:

Amplifier: input jack and gain control

located on synchroscope panel.

Power Supply: on-off switch mounted inside synchroscope. If this switch is left on a-c power may be con

is left on, a-c power may be controlled by the synchroscope on-off

switch.

#### References

Instruction Manual: R-164
Amplifier Circuit Schematic: B-33501
Power Supply Circuit Schematic: B-33357